ABSTRACT OF THE DISCLOSURE

A synchronous memory device and methods of operation and controlling such a device. The synchronous memory device includes input receiver circuitry to sample a first operation code synchronously with respect to an external clock signal. The synchronous memory device also includes a programmable register to store a binary value in response to the first operation code, wherein the binary value is representative of an amount of time to transpire before the memory device outputs data. The synchronous memory device also includes output driver circuitry to output data in response to a second operation code and after the amount of time transpires. A first portion of data is output synchronously with respect to a first transition of the external clock signal and a second portion of data is output synchronously with respect to a second transition of the external clock signal.